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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,437	12/05/2003	James M. Cleeves	SAND-01209US0	9392

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
06/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,437	CLEEVES ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-13 and 15-59* is/are pending in the application.

4a) Of the above claim(s) *19-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12,13 and 15-18* is/are rejected.

7)☐ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed March 6, 2007.

Response to Arguments

2. Applicant's arguments with respect to claims 1-8, 10-13 and 15-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (U.S. Patent No. 4,498,226).

In regards to claim 1, Inoue et al. ("Inoue") discloses the following:

a) a substrate device level comprising substrate transistors (T1, T3, T4), the substrate transistors having a substrate pitch, some portion of each of the substrate transistors formed in a monocrystalline substrate (1) (For Example: See Figure 1 and Abstract); and

b) a first above substrate device level formed above the substrate device level, the first above device level comprising first above-substrate devices having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch (For Example: See Figure 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 3, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. Patent No. 4,498,226) in view of Kleveland et al. (U.S. Patent No. 6,631,085).

In regards to claim 2, Inoue fails to disclose the following:

a) the first above-substrate devices of the first above substrate device level comprises a first plurality of memory cells, the memory cells at the first above-substrate pitch.

However, Kleveland et al. ("Kleveland") discloses the first above substrate device level comprises a first plurality of memory cells (56 and 58) (For Example: See Abstract and Figure 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include the first above substrate device level comprises a first plurality of memory cells as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Inoue and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Inoue.

In regards to claim 3, Inoue fails to disclose the following:

a) the first above substrate device level comprises a driver circuitry.

However, Kleveland discloses the first above substrate device level comprises driver circuitry (For Example: See Figure 12 and Column 8 Lines 64-66). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include the first above substrate device level comprises a first above substrate device level comprises driver circuitry as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Owada and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Inoue.

In regards to claim 12, Inoue fails to disclose the following:

a) the plurality of memory cells form part of a monolithic three dimensional memory array.

However, Kleveland discloses the plurality of memory cells form part of a monolithic three dimensional memory array (For Example: See Figure 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include a plurality of memory cells that form part of a monolithic three dimensional memory array as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Inoue and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Inoue.

In regards to claim 15, Inoue fails to disclose the following:

a) the memory cells are passive element memory cells.

However, Kleveland discloses memory cells that are passive element memory cells (For Example: See Column 15 Lines 41-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include memory cells that are passive element memory cells as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Inoue and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Inoue.

In regards to claim 16, Inoue fails to disclose the following:

a) the memory cells are antifuse diode cells.

However, Kleveland discloses memory cells that are antifuse diode cells (For Example: See Column 4 Lines 24-36). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include memory cells that are antifuse diode cells as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Inoue and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Inoue.

7. Claims 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. Patent No. 4,498,226) in view of Kleveland et al. (U.S. Patent No. 6,631,085) and Cleeves et al. (U.S. Patent No. 6,486,066).

In regards to claim 4, Inoue fails to disclose the following:

a) a first area, said area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch.

However, Cleeves et al. ("Cleeves") discloses a first area (202) comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area (204) having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch (For Example: See Figure 2B). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include a first area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch as disclosed in Cleeves because it aids in providing uniform device density (For Example: See Column 6 Lines 24-28).

Additionally, since Inoue and Cleeves are both from the same field of endeavor, the purpose disclosed by Cleeves would have been recognized in the pertinent art of Inoue.

In regards to claim 5, Inoue fails to disclose the following:

a) the first area comprises a plurality of substantially parallel, substantially coplanar rails.

However, Kleveland discloses that the first area comprises a plurality of substantially parallel, substantially coplanar rails (For Example: See Figure 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the

semiconductor of Inoue to include that the first area comprises a plurality of substantially parallel, substantially coplanar rails as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Inoue and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Inoue.

In regards to claim 6, Inoue fails to disclose the following:

a) photolithography processes are optimized to minimize the first above substrate pitch of the plurality of rails in the first area.

However, the following limitation makes it a product by process claim: a) "photolithography processes are optimized to minimize the first above substrate pitch of the plurality of rails in the first area." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in

"product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 7, Inoue fails to disclose the following:

a) the plurality of rails is patterned using off-axis illumination.

However, the following limitation makes it a product by process claim: a) "patterned using off-axis illumination." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 8, Inoue fails to disclose the following:

a) the plurality of rails is patterned using a dipole illumination aperture.

However, the following limitation makes it a product by process claim: a) "patterned using a dipole illumination aperture." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 9, Inoue fails to disclose the following:

a) a die includes dummy structures.

However, Cleeves discloses a die including dummy structures (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include a die including dummy structures as disclosed in Cleeves because it aids in enhancing chemical mechanical planarization (For Example: See Column 1 Lines 28-31).

Additionally, since Inoue and Cleeves are both from the same field of endeavor, the purpose disclosed by Cleeves would have been recognized in the pertinent art of Inoue.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. Patent No. 4,498,226) in view of Kleveland et al. (U.S. Patent No. 6,631,085) and Mitsubishi Electric (Japanese Publication No. 3393923).

In regards to claim 13, Inoue fails to disclose the following:

a) memory array comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line.

However, Mitsubishi discloses a memory array that comprises segmented bit lines and global bit lines, wherein two segmented bit lines (SBL1 and SBL2) share a vertical connection to an associated global bit line (GBL1) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include memory array that comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line as disclosed in Mitsubishi because it aids in reducing power consumption (For Example: See Abstract).

Additionally, since Inoue and Mitsubishi are both from the same field of endeavor, the purpose disclosed by Mitsubishi would have been recognized in the pertinent art of Inoue.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. Patent No. 4,498,226) in view of Kleveland et al. (U.S. Patent No. 6,631,085) and Pio (U.S. Publication No. 2003/0198101).

In regards to claim 14, Inoue fails to disclose the following:

a) the memory array comprises word lines segments and a word line driver circuit in the substrate.

However, Pio discloses a memory array that comprises word lines segments and a word line driver circuit in the substrate (For Example: See Page 6-Claim 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include a memory array that comprises word lines segments and a word line driver circuit in the substrate as disclosed in Pio because it aids in preventing stored data from being erased (For Example: See Paragraph 15).

Additionally, since Inoue and Pio are both from the same field of endeavor, the purpose disclosed by Pio would have been recognized in the pertinent art of Inoue.

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. Patent No. 4,498,226) in view of Kleveland et al. (U.S. Patent No. 6,631,085) and Young (U.S. Patent No. 5,621,683).

In regards to claim 17, Inoue fails to disclose the following:

a) the memory cells are thin film transistors having a charge-storage dielectric.

However, Young discloses memory cells that are thin film transistors having a charge-storage dielectric (For Example: See Column 4 Lines 35-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor

of Inoue to include memory cells that are thin film transistors having a charge-storage dielectric as disclosed in Young because they aid in reducing costs (For Example: See Column 3 Lines 34-38).

Additionally, since Inoue and Young are both from the same field of endeavor, the purpose disclosed by Young would have been recognized in the pertinent art of Inoue.

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. Patent No. 4,498,226) in view of Kleveland et al. (U.S. Patent No. 6,631,085), Young (U.S. Patent No. 5,621,683) and Nakai (U.S. Patent No. 5,587,948).

In regards to claim 18, Inoue fails to disclose the following:

a) the memory cells are arranged in series-connected NAND strings.

However, Nakai discloses memory cells that are arranged in series-connected NAND strings (For Example: See Column 3 Lines 40-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Inoue to include are arranged in series-connected NAND strings as disclosed in Nakai because it aids in extending the life of the chip (For Example: See Column 2 Lines 53-60).

Additionally, since Inoue and Nakai are both from the same field of endeavor, the purpose disclosed by Nakai would have been recognized in the pertinent art of Inoue.

12. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,266,511) in view of Silicon Processing by Wolf et al.

In regards to claim 1, Takao discloses the following:

a) a substrate device level comprising substrate transistors, the substrate transistors having a substrate pitch, some portion of each of the substrate transistors formed in a substrate (1) (For Example: See Figure 1); and

b) a first above substrate device level formed above the substrate device level, the first above device level comprising first above-substrate devices having a first above-substrate pitch, wherein the first above-substrate pitch is smaller than the substrate pitch (For Example: See Figure 7).

In regards to claim 1, Takao fails to disclose the following:

a) a monocrystalline substrate.

However, Wolf et al. ("Wolf") discloses a monocrystalline substrate (For Example: See Page 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include a monocrystalline substrate as disclosed in Wolf because it is commonly utilized as the starting material (For Example: See Page 1).

Additionally, since Takao and Wolf are both from the same field of endeavor, the purpose disclosed by Wolf would have been recognized in the pertinent art of Takao.

13. Claims 2, 3, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,266,511) in view of Silicon Processing by Wolf et al. and Kleveland et al. (U.S. Patent No. 6,631,085).

In regards to claim 2, Takao fails to disclose the following:

a) the first above-substrate devices of the first above substrate device level comprises a first plurality of memory cells, the memory cells at the first above-substrate pitch.

However, Kleveland et al. ("Kleveland") discloses the first above substrate device level comprises a first plurality of memory cells (56 and 58) (For Example: See Abstract and Figure 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include the first above substrate

device level comprises a first plurality of memory cells as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Takao and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Takao.

In regards to claim 3, Takao fails to disclose the following:

a) the first above substrate device level comprises a driver circuitry.

However, Kleveland discloses the first above substrate device level comprises driver circuitry (For Example: See Figure 12 and Column 8 Lines 64-66). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include the first above substrate device level comprises a first above substrate device level comprises driver circuitry as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Takao and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Takao.

In regards to claim 12, Takao fails to disclose the following:

a) the plurality of memory cells form part of a monolithic three dimensional memory array.

However, Kleveland discloses the plurality of memory cells form part of a monolithic three dimensional memory array (For Example: See Figure 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include a plurality of memory cells that form part of a monolithic

three dimensional memory array as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Takao and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Takao.

In regards to claim 15, Takao fails to disclose the following:

a) the memory cells are passive element memory cells.

However, Kleveland discloses memory cells that are passive element memory cells (For Example: See Column 15 Lines 41-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include memory cells that are passive element memory cells as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Takao and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Takao.

In regards to claim 16, Takao fails to disclose the following:

a) the memory cells are antifuse diode cells.

However, Kleveland discloses memory cells that are antifuse diode cells (For Example: See Column 4 Lines 24-36). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include memory cells that are antifuse diode cells as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Takao and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Takao.

14. Claims 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,266,511) in view of Silicon Processing by Wolf et al., Kleveland et al. (U.S. Patent No. 6,631,085) and Cleeves et al. (U.S. Patent No. 6,486,066).

In regards to claim 4, Takao fails to disclose the following:

a) a first area, said area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch.

However, Cleeves et al. ("Cleeves") discloses a first area (202) comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area (204) having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch (For Example: See Figure 2B). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include a first area comprising portions of the first plurality of memory cells, the memory cells having the first above-substrate pitch and a second area having a fan out pitch, wherein said fan-out pitch is larger than the first above-substrate pitch as disclosed in Cleeves because it aids in providing uniform device density (For Example: See Column 6 Lines 24-28).

Additionally, since Takao and Cleeves are both from the same field of endeavor, the purpose disclosed by Cleeves would have been recognized in the pertinent art of Takao.

In regards to claim 5, Takao fails to disclose the following:

a) the first area comprises a plurality of substantially parallel, substantially coplanar rails.

However, Kleveland discloses that the first area comprises a plurality of substantially parallel, substantially coplanar rails (For Example: See Figure 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include that the first area comprises a plurality of substantially parallel, substantially coplanar rails as disclosed in Kleveland because it aids in providing low cost high density semiconductor memories (For Example: See Column 1 Lines 20-27).

Additionally, since Takao and Kleveland are both from the same field of endeavor, the purpose disclosed by Kleveland would have been recognized in the pertinent art of Takao.

In regards to claim 6, Takao fails to disclose the following:

a) photolithography processes are optimized to minimize the first above substrate pitch of the plurality of rails in the first area.

However, the following limitation makes it a product by process claim: a) "photolithography processes are optimized to minimize the first above substrate pitch of the plurality of rails in the first area." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289

(CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 7, Takao fails to disclose the following:

a) the plurality of rails is patterned using off-axis illumination.

However, the following limitation makes it a product by process claim: a) "patterned using off-axis illumination." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 8, Takao fails to disclose the following:

a) the plurality of rails is patterned using a dipole illumination aperture.

However, the following limitation makes it a product by process claim: a) "patterned using a dipole illumination aperture." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 9, Takao fails to disclose the following:

a) a die includes dummy structures.

However, Cleeves discloses a die including dummy structures (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include a die including dummy

structures as disclosed in Cleeves because it aids in enhancing chemical mechanical planarization (For Example: See Column 1 Lines 28-31).

Additionally, since Takao and Cleeves are both from the same field of endeavor, the purpose disclosed by Cleeves would have been recognized in the pertinent art of Takao.

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,266,511) in view of Silicon Processing by Wolf et al., Kleveland et al. (U.S. Patent No. 6,631,085) and Mitsubishi Electric (Japanese Publication No. 3393923).

In regards to claim 13, Takao fails to disclose the following:

a) memory array comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line.

However, Mitsubishi discloses a memory array that comprises segmented bit lines and global bit lines, wherein two segmented bit lines (SBL1 and SBL2) share a vertical connection to an associated global bit line (GBL1) (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include memory array that comprises segmented bit lines and global bit lines, wherein two segmented bit lines share a vertical connection to an associated global bit line as disclosed in Mitsubishi because it aids in reducing power consumption (For Example: See Abstract).

Additionally, since Takao and Mitsubishi are both from the same field of endeavor, the purpose disclosed by Mitsubishi would have been recognized in the pertinent art of Takao.

16. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,266,511) in view of Silicon Processing by Wolf et al., Kleveland et al. (U.S. Patent No. 6,631,085) and Pio (U.S. Publication No. 2003/0198101).

In regards to claim 14, Takao fails to disclose the following:

a) the memory array comprises word lines segments and a word line driver circuit in the substrate.

However, Pio discloses a memory array that comprises word lines segments and a word line driver circuit in the substrate (For Example: See Page 6-Claim 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include a memory array that comprises word lines segments and a word line driver circuit in the substrate as disclosed in Pio because it aids in preventing stored data from being erased (For Example: See Paragraph 15).

Additionally, since Takao and Pio are both from the same field of endeavor, the purpose disclosed by Pio would have been recognized in the pertinent art of Takao.

17. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,266,511) in view of Silicon Processing by Wolf et al., Kleveland et al. (U.S. Patent No. 6,631,085) and Young (U.S. Patent No. 5,621,683).

In regards to claim 17, Takao fails to disclose the following:

a) the memory cells are thin film transistors having a charge-storage dielectric.

However, Young discloses memory cells that are thin film transistors having a charge-storage dielectric (For Example: See Column 4 Lines 35-60). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor

of Takao to include memory cells that are thin film transistors having a charge-storage dielectric as disclosed in Young because they aid in reducing costs (For Example: See Column 3 Lines 34-38).

Additionally, since Takao and Young are both from the same field of endeavor, the purpose disclosed by Young would have been recognized in the pertinent art of Takao.

18. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takao et al. (U.S. Patent No. 5,266,511) in view of Silicon Processing by Wolf et al., Kleveland et al. (U.S. Patent No. 6,631,085), Young (U.S. Patent No. 5,621,683) and Nakai (U.S. Patent No. 5,587,948).

In regards to claim 18, Takao fails to disclose the following:

a) the memory cells are arranged in series-connected NAND strings.

However, Nakai discloses memory cells that are arranged in series-connected NAND strings (For Example: See Column 3 Lines 40-45). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Takao to include are arranged in series-connected NAND strings as disclosed in Nakai because it aids in extending the life of the chip (For Example: See Column 2 Lines 53-60).

Additionally, since Takao and Nakai are both from the same field of endeavor, the purpose disclosed by Nakai would have been recognized in the pertinent art of Takao.

Allowable Subject Matter

19. Claims 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

ML

May 21, 2007

MONICA LEWIS
PRIMARY PATENT EXAMINER